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Attorney Docket No. 42390.P9429

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: )  
Jin Yang )  
Application No. 09/608,637 )  
Filed: June 30, 2000 )  
For: **METHODS FOR FORMAL** )  
**VERIFICATION ON A** )  
**SYMBOLIC LATTICE DOMAIN** )

Examiner: \*\*\*

Art Unit: 2763

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Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered, and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.	
By: <u>Anne Collette</u> Anne Collette	Date: <u>3/8/2004</u>



Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

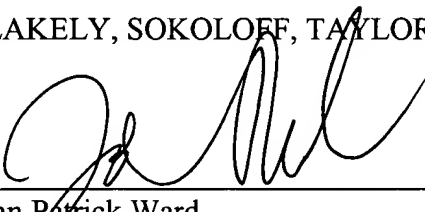
- X   37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
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If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3/5/04

  
\_\_\_\_\_  
John Patrick Ward  
Reg. No. 40,216

12400 Wilshire Blvd.  
Seventh Floor  
Los Angeles, CA 90025-1030  
(408) 720-8300

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 42390.P9429	Application Number: 09/608,637
Sheet 1 of 1		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2763

**OTHER ART - NO PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation <sup>2</sup>
		BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998	
		BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424	
		CAMPOS, S.V.A., "Symbolic Model Checking in Practice," <u>XII Symposium on Integrated Circuits and Systems Design</u> , 1999 Natal, Brazil - IEEE, September 1999, pp. 98-101	
		HOJATI, R., et al., "Early Quantification and Partitioned Transition Relations," <u>1999 IEEE International Conference on Computer Design: VLSI in Computers and Processors</u> , 1996, ICCD '96 Proceedings - Austin, TX, October, 1996, pp. 12-19	
		ZHANG, ZHANG, "An Approach to Hierarchy Model Checking via Evaluating CTL Hierarchically," <u>Proceedings of the Fourth Asian Test Symposium</u> , 1995 - Bangalore, India, November 1995, pp. 45-49	

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